A 94-GHz 0.35-W Power Amplifier Module

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***Abstract*— This paper presents a 94-GHz power amplifier (PA) module. This module contains three identical monolithic microwave integrated circuit (MMIC) PA chips and demonstrates 0.35-W output power at the waveguide output port with a miniature size. The MMIC PA is a two-stage monolithic W-band PA using 0.1-μm pseudomorphic AlGaAs/InGaAs/GaAs T-gate power high electron mobility transistor (HEMT) process. This MMIC PA exhibits a measured linear gain of 8 dB and a maximum output power of 300 mW with 10.5% peak power-added efficiency (PAE) at 94 GHz. To our knowledge, both the 300-mW output power MMIC PA and the 0.35-W PA module represent the highest output power amplification component performance at this frequency.**

***Index Terms*—HEMT, MMIC, PA.**

I. Introduction

The next generation millimeter-wave (MMW) systems require high-performance, reliable, and low-cost components. Monolithic MMW integrated circuits (MMIC's) have great potential to meet such requirements over the conventional hybrid integrated circuit approach. The frequency of interest for missile-seeker radar, communications, smart weapon, electronic warfare, and radiometry system applications is 94 GHz. A miniature 94-GHz power amplifier (PA) module is attractive for transmitter application in W-band missile seekers and phased array radars. In the past, the transmitter components in this frequency were usually based on IMPATT diodes and suffered from size constraints as well as dc power consumption.

Great effort has been devoted to the development of monolithic integrated circuits for MMW applications recently. In the earlier time, due to lack of 94-GHz MMIC amplifiers, MMIC-based 94-GHz transmitter modules using frequency multiplication device approaches were proposed (frequency trippler approach, but no test results cited) [1] or implemented (doubler approach, demonstrated 90-mW output power) [2]. These approaches not only require more components, for example, lower frequency PA's and frequency multipliers with 94-GHz output, resulting in a higher cost, but also suffer by the loss of frequency multiplication and consequently lead to higher dc power consumption. Various W-band MMIC low-noise amplifiers [3], [4] and power amplifiers [5]–[8] have been successfully demonstrated using an AlGaAs/InGaAs/GaAs pseudomorphic T-gate power high electron mobility transistor (HEMT) with 0.1-μm gate length. Output power capability for W-band amplifiers has been demonstrated and enhanced in the past few years [5]–[8]. Using these MMIC amplifiers, a PA module delivering 100-mW output power has been reported [11].

This paper presents the development of a 94-GHz two-stage monolithic PA using the 0.1-μm power HEMT process on a thinned 2-mil GaAs substrate and a 0.35-W PA module utilizing three of the MMIC PA chips. The main advantages of a thinner substrate are lower thermal resistance and the use of smaller via holes, which results in the design of a more compact PA than those using 4-mil substrate. At 94 GHz, the MMIC PA exhibits 8-dB linear gain and 300-mW maximum output power with 10.5% peak efficiency at the chip microstrip-line output port. This performance demonstrates the latest breakthrough of the output power capability for a W-band MMIC amplifier. A 94-GHz PA miniature module is further developed using one of the MMIC chips to drive another two chips with a pair of Wilkinson power combiners on quartz substrates. This PA module achieves a measured output power of 0.35 W at the waveguide output port with a size of 1”×0.6’’×0.3”, which also represents the state-of-the-art performance of MMIC-based W-band PA modules.

II. Device Characteristics and Modeling

The 0.1-μm power HEMT device development has been reported in the previous publication [9]. The major difference for the amplifier presented here is that it is processed on a 2-mil substrate. MMIC power amplifiers using 2-mil substrates have been successfully demonstrated at lower frequencies [10]. Using a thinner substrate allows for smaller via holes and lower thermal resistance. With smaller via holes, device sources can be grounded with separate via holes, thus lowering the source inductance, which in turn improves the gain and power density. The multifinger gate HEMT device finger spacing in this compact device layout is also reduced in order to minimize parasitics. The unity current gain frequency (f_T) and maximum oscillation frequency ($f_{\max}$) of this device are 200 and 130 GHz, respectively.

The device linear model is developed by carefully fitting the FET equivalent circuit to measured small-signal S-parameters to 50 GHz. Measured dc I–V data are used together with linear model elements to complete the Curtice–Ettenberg FET asymmetric model for predicting output power performance [12]. The device linear and nonlinear model for an eight-finger

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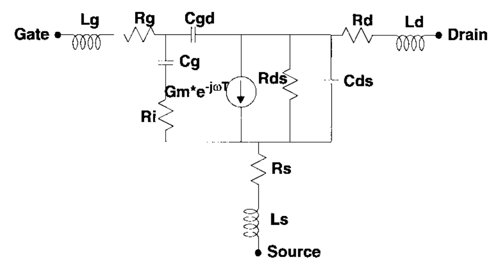
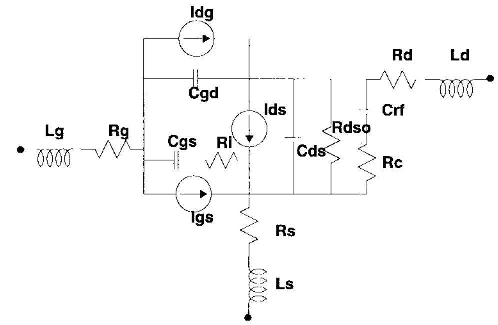


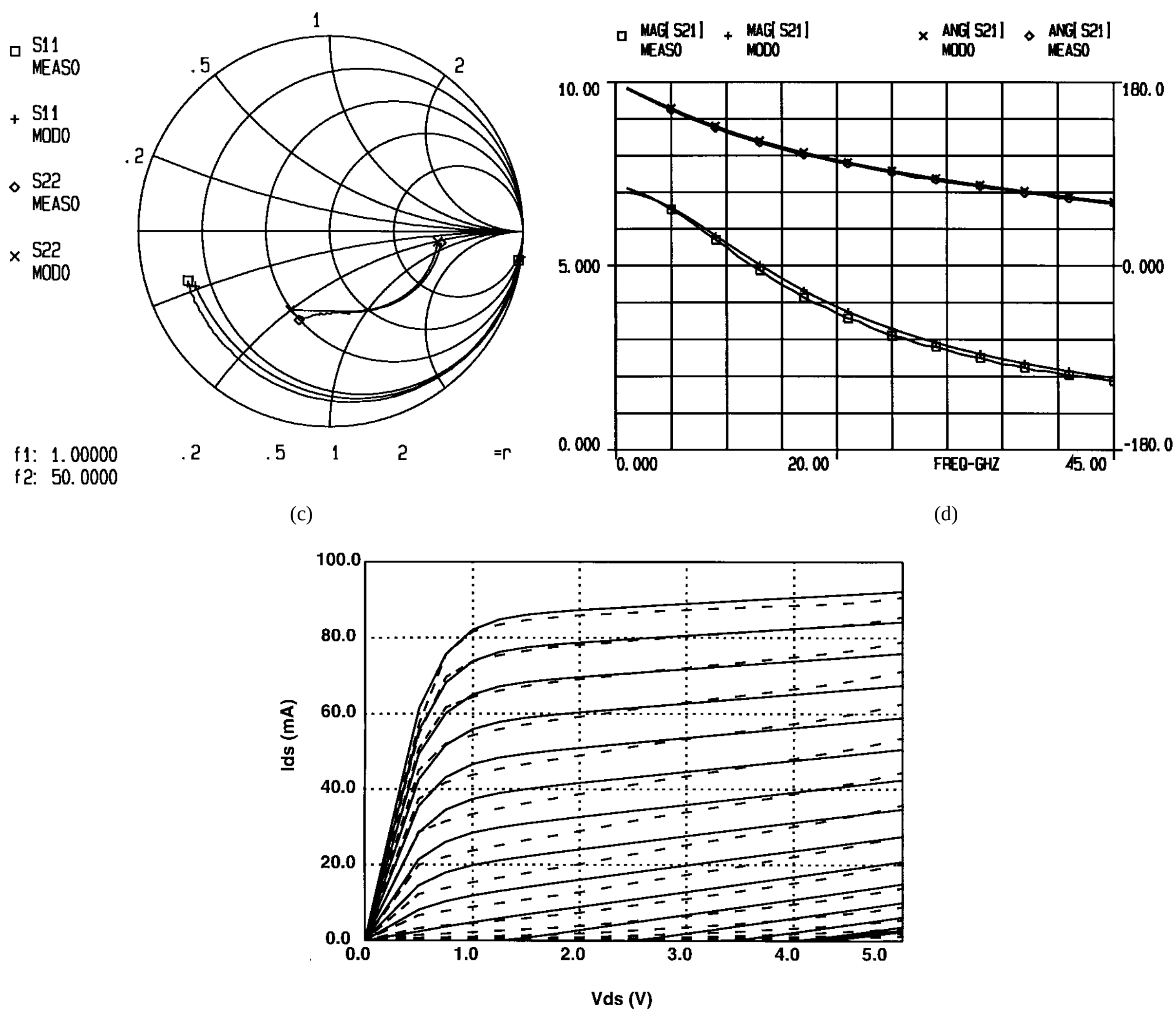
Gm (mS)	T (ps)	Cgs (pF)	Cgd (pF)	Cds (pF)	Rds (Ω)	Ri (Ω)	Rg (Ω)	Rd (Ω)	Rs (Ω)	Lg (nH)	Ld (nH)	Ls (nH)
0.095	0.65	0.135	0.0174	0.047	170	0.73	1.2	0.7	0.5	0.02	0.016	0.0004

(a)



$a_0 = 0.4309E\text{-}01$ A, $a_1 = 0.9153E\text{-}1$ A/V, $a_2 = 0.2149E\text{-}1$ A/V^2,
$a_3 = -0.2996E\text{-}1$ A/V^3, $\beta = 0.36842E\text{-}1$ V^{-1}, $\gamma = 2.1081$ V^{-1}, Rdso = 296 Ω

(b)

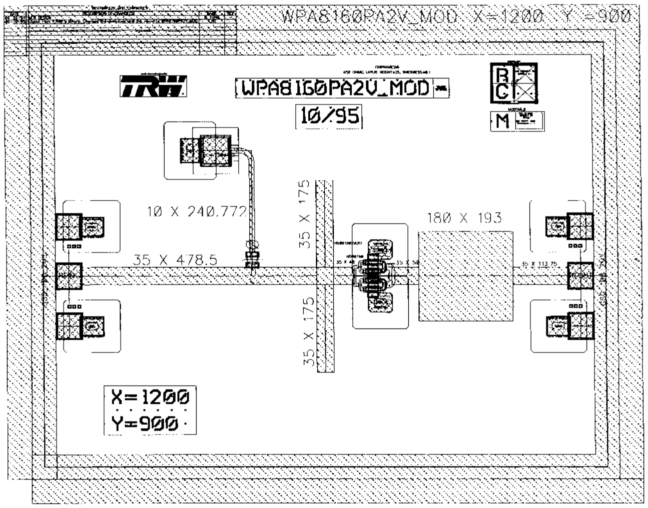


(c) (d)

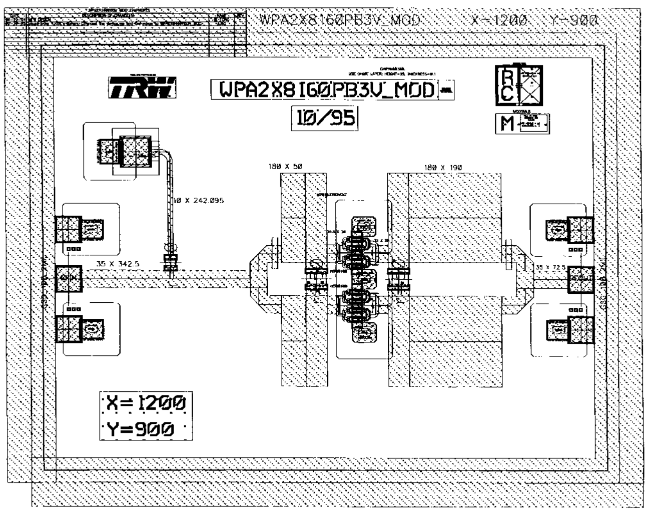
(e)

Fig. 1. (a) Linear equivalent circuit model and parameters of an eight-finger 160-μm HEMT. (b) Curtice–Ettenberg FET asymmetric equivalent circuit model and parameters of an eight-finger 160-μm HEMT. (c) Measured and modeled $S_{1}1$ and $S_{2}2$ of the device from 1 to 50 GHz. MEAS0 is the measured data and MOD0 is the model. (d) Measured and modeled $S_{2}1$ (magnitude and angle) of the device from 1 to 50 GHz. MEAS0 is the measured data and MOD0 is the model. (e) Measured (dashed line) and simulated (solid line) *I–V* characteristics of an eight-finger 160-μm HEMT.

160-μm total gate-width HEMT device and the measured S-parameters together with dc I–V data compared with the model are shown in Fig. 1. In addition, simple prematched structures with small-signal gain frequency response centered at 94 GHz for a single device and two devices in parallel are also designed as shown in Fig. 2. These test structures are used to verify the validity of the device model at W-band. Fig. 3 shows the measured results and simulated performance from 75 to 110 GHz using the device linear model of the prematched structures. Reasonable agreement is observed for



(a)



(b)

Fig. 2. (a) Layout of the single-device prematched test structure. (b) Layout of the two-device prematched test structure.

both of the test structures. As can be observed, the discrepancy between simulation and measurement in small-signal gain is within 1 dB at the frequency of interest.

III. Monolithic Power Amplifier Design and Performance

The power amplifier is a single-ended two-stage design with a compact chip size. The compact chip design features include compact device layout, dry etch via, and narrow line width for low characteristic impedance on the 2-mil substrate (compared with the conventional 4-mil design [5]–[8]). The chip photograph is shown in Fig. 4 with a chip size of only 2.3×1.8 mm. The first stage employs four cells of eight-finger 160-μm HEMT devices and second stage has twice the device periphery with eight HEMT devices. The RF performance is optimized with reactive matching elements. The microstrip-line edge-coupled lines between both stages provide proper impedance transformation, which produces a wide-band design and ensures performance repeatability. After the matching elements are determined, full-wave electromagnetic (EM) analysis [15] is used for the passive structures to eliminate the uncertainties caused by the quasistatic models.

With metal–insulator–metal (MIM) capacitors for dc blocking, radial stubs for RF bypass, and shunt R–C in the biasing networks for low frequency stability, the chip is made to be on-wafer probable. A small resistor and a shunt quarter-wavelength short stub are placed in the input and output matching networks to remove the undesired out-of-band gain. Isolation resistors between every pair of paralleled devices are used to prevent possible oscillations due to the high transconductance (g_m) of a large device periphery.

The PA was first tested on-wafer for dc screening and linear gain. Owing a large part to the GaAs process maturity, very high RF yield was achieved. On a single wafer where 11 sites of PA are available, ten sites show 7–10-dB linear gain from 88 to 94 GHz. The bias voltages for drain and gate are 4 and 0 V, respectively. Fig. 5 shows the on-wafer tested linear gain performance from 75 to 110 GHz of all ten sites from a single wafer. The PA chip was then tested in a WR-10 waveguide test-fixture with a fin-line waveguide-to-microstrip-line transition for output power measurement at the same bias condition. As shown in Fig. 6, the PA exhibits a 24.8-dBm (300-mW) maximum output power with a power gain of 4 dB and a peak power-added efficiency (PAE) of 10.5% at 94 GHz. With a slight decrease in output power, PAE can be improved to 12.2% by lowering the drain voltage on the first stage to 3 V with a maximum output power of 24.6 dBm. All of the power data presented here are the power levels at the chip end microstrip-line output port and have accounted for a 0.7-dB loss for each transition.

IV. 94-GHz Module Design and Measurement Results

The block diagram of this PA module is shown in Fig. 7. This module includes three identical 94-GHz PA chips, described in Section III. One serves as the driver amplifier and a pair of Wilkinson power combiners are used to combine another two PA chips for output power. The module housing is made of an alloyed composite material (60% Al and 40% Si, commonly referred as A40), and with a size of 1”× 0.6’’×0.3’’. The main selection of this material is mainly due to the coefficient of thermal expansion (CTE) to be matched with GaAs substrate and its thermal property. The input and output ports are WR-10 waveguides and E-plane probe transitions on 5-mil-thick quartz substrates are used to couple the RF power to 50-Ω microstrip lines. The probe design is similar to those reported at lower frequencies (26–110 GHz) [13]. Another full-wave EM analysis software [14] is used for the design and the measured insertion loss is about 0.5 dB per transition at 94 GHz. The Wilkinson power combiner is designed on 5-mil quartz substrate using full-wave EM analysis [15]. The measured insertion loss of a pair of the combiner (back-to-back) is 1.8 dB (corrected with transition loss) with return loss of better than 10 dB from 88 to 100 GHz, as shown in Fig. 8. All of the substrates were mounted on the housing using silver epoxy, and 2-mil-wide gold ribbon

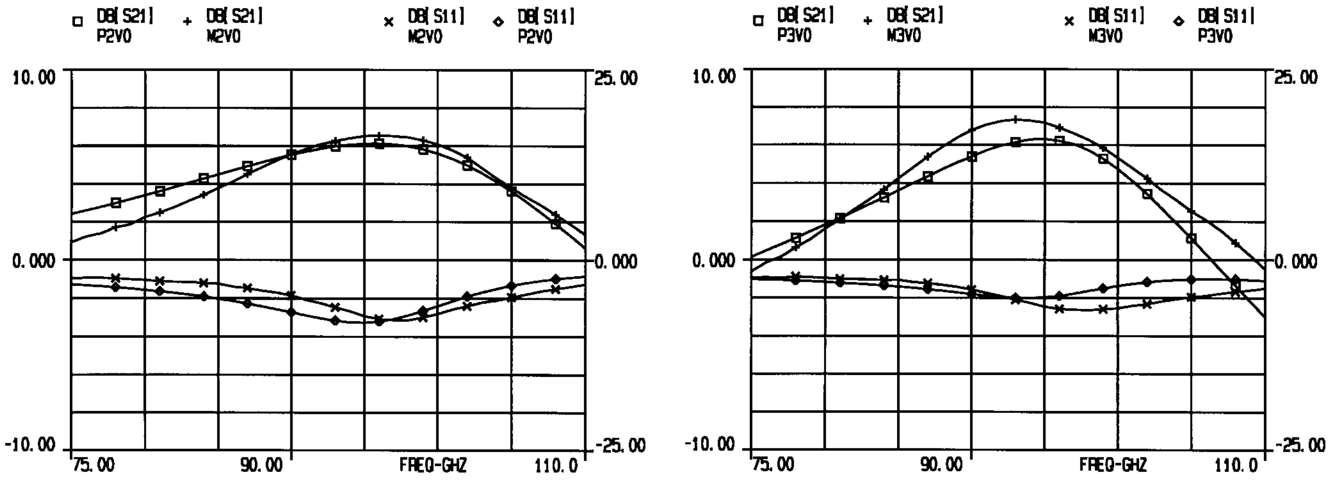


Fig. 3 (a) Validation of the device model with the single-device test structure. (b) Validation of the device model with the two-device test structure.

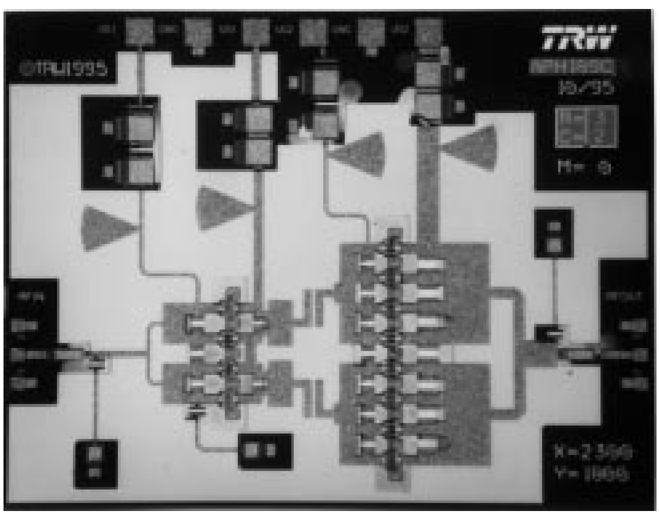


Fig. 4. Photograph of the W-band monolithic power amplifier.

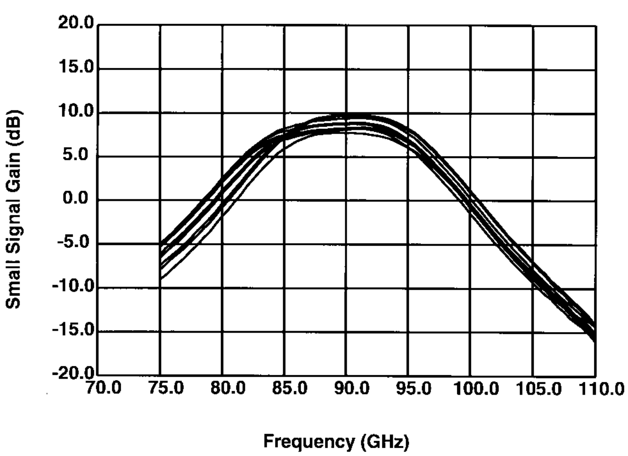


Fig. 5. Small-signal gain of ten different sites from a single wafer.

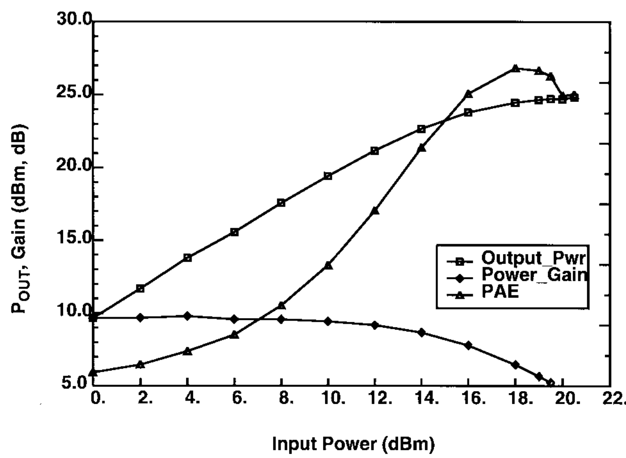


Fig. 6. Measured output power and power-added efficiency at 94 GHz.

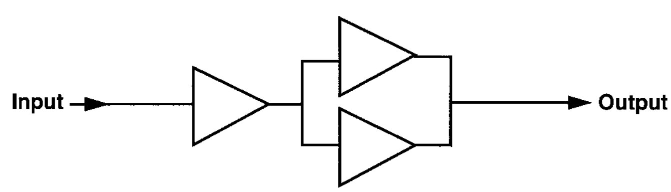


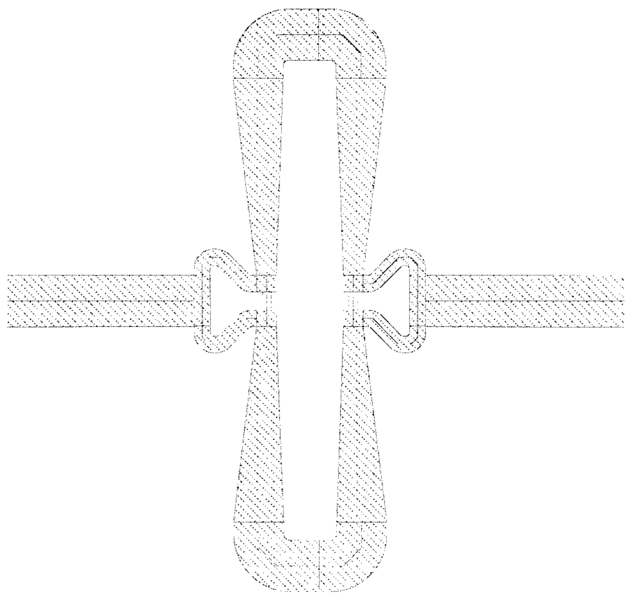
Fig. 7. Block diagram of the W-band power module.

was thermally bonded for good electrical contact to connect the quartz substrates and GaAs chips.

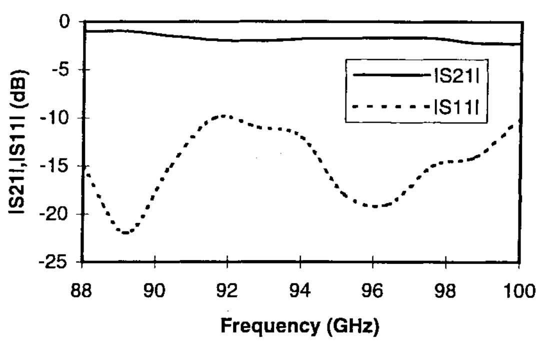
Fig. 9 is the photograph of the complete miniature PA module. This module exhibits a measured output power of 0.35-W at output waveguide port at 94-GHz with a power gain of 8 dB and a PAE of 5%. The output power versus input power curve is plotted in Fig. 10. As indicated in the curve, the linear power gain of this module is 13 dB. During the testing, the drain bias voltage of the HEMT devices on the PA chips are all at 4 V with gate bias at 0 V with a total drain current of 1.58 A.

V. Summary

We have demonstrated a W-band MMIC two-stage power amplifier using a 0.1-μm AlGaAs/InGaAs/GaAs power HEMT process on a 2-mil GaAs substrate. Excellent RF yield based on small-signal gain, 300-mW output power, and greater



(a)



(b)

Fig. 8. (a) Back-to-back drawing of the combiner. (b) Measurement of the back-to-back combiner.

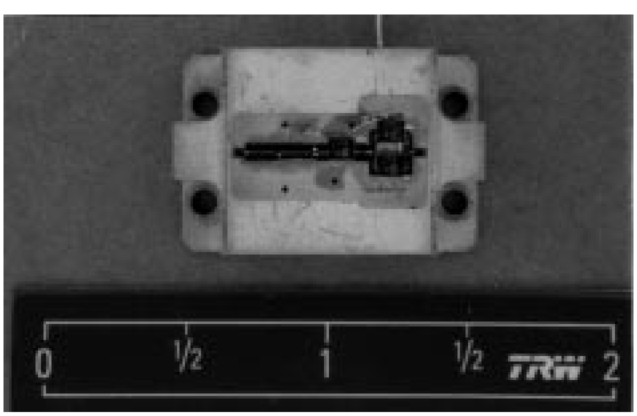


Fig. 9. Photograph of the W-band 300-mW power module.

than 10% peak PAE have been achieved. This performance represents a breakthrough in monolithic millimeter-wave PA design at 94 GHz and demonstrates the maturity of power HEMT process capability. A 94-GHz power amplifier module is further developed using this W-band MMIC PA chip and exhibits 0.35-W output power from the waveguide output port.

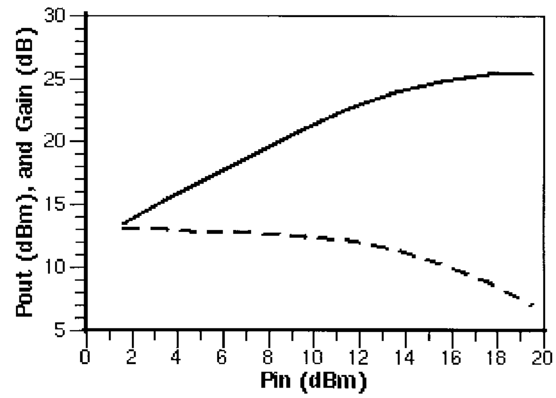


Fig. 10. Measured P_{IN}–P_{OUT} at 94 GHz of the W-band power module.

This is also the best output power performance among the reported MMIC-based transmitter modules at this frequency.

ACKNOWLEDGMENT

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Yonghui Shu, (M'92) photograph and biography not available at the time of publication.

Gee S. Dow, (S'78–M'83) photograph and biography not available at the time of publication.

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